FORM PTO-1390 (Modified) (REV 11-98) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER	
L9289.01101	
U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR	
Unassigned	09/744338
INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE
PCT/JP00/03446	May 30, 2000
PRIORITY DATE CLAIMED	
May 31, 1999	

TITLE OF INVENTION

RECEPTION APPARATUS AND EQUALIZING PROCESSING METHOD

APPLICANT(S) FOR DO/EO/US

Yoshiko SAITO
Mitsuru UESUGI

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. ☐ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☒ A copy of the International Search Report (PCT/ISA/210).
8. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.
9. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
10. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
11. ☐ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).

Items 13 to 20 below concern document(s) or information included:

13. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
14. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☐ A **FIRST** preliminary amendment.
16. ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
17. ☐ A substitute specification.
18. ☐ A change of power of attorney and/or address letter.
19. ☐ Certificate of Mailing by Express Mail
20. ☒ Other items or information:

Claim for Priority with PCT/IB/304
PCT/IB/308
PCT/RO/101

JC07 Rec'd PCT/PTO 23 JAN 2001

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR) Unassigned 09/744558	INTERNATIONAL APPLICATION NO. PCT/JP00/03446	ATTORNEY'S DOCKET NUMBER L9289.01101

21. The following fees are submitted:.

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :		CALCULATIONS PTO USE ONLY
☐ Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2) paid to USPTO and International Search Report not prepared by the EPO or JPO	$1,000.00	
☒ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO	$860.00	
☐ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO	$710.00	
☐ International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4)	$690.00	
☐ International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4)	$100.00	
ENTER APPROPRIATE BASIC FEE AMOUNT =		$860.00
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).		$0.00

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	
Total claims	8 - 20 =	0	x $18.00	$0.00
Independent claims	4 - 3 =	1	x $80.00	$80.00
Multiple Dependent Claims **(check if applicable)**.			☐	$0.00
TOTAL OF ABOVE CALCULATIONS			=	$940.00
Reduction of 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also be filed (Note 37 CFR 1.9, 1.27, 1.28) **(check if applicable).**			☐	$0.00
SUBTOTAL			=	$940.00
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (f)).			+	$0.00
TOTAL NATIONAL FEE			=	$940.00
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) **(check if applicable).**			☒	$40.00
TOTAL FEES ENCLOSED			=	$980.00
			Amount to be: refunded	$
			charged	$

☒ A check in the amount of **$980.00** to cover the above fees is enclosed.

☐ Please charge my Deposit Account No. in the amount of to cover the above fees.
A duplicate copy of this sheet is enclosed.

☒ The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. **19-4375** A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

James E. Ledbetter, Esq.
STEVENS, DAVIS, MILLER & MOSHER, LLP
1615 L Street, N.W., Suite 850
Washington, DC 20036
Tel: 202-408-5100
Fax: 202-408-5200

SIGNATURE

James E. Ledbetter
NAME

28,732
REGISTRATION NUMBER

January 19, 2001
DATE

DESCRIPTION

RECEPTION APPARATUS AND EQUALIZING PROCESSING METHOD

Technical Field

The present invention relates to a reception apparatus and equalizing processing method, and more particularly, to a reception apparatus and equalizing processing method that update on demand tap coefficients of an equalizer based on an adaptive algorithm.

Background Art

A conventional reception apparatus converges received signal components spread over a time axis into a range, which is timewise short as possible, enabling compensation of an equalizer, prior to equalizing processing.

The conventional reception apparatus is explained below using FIGs.1 to 6. FIG.1 is a partial block diagram illustrating a schematic configuration of the conventional reception apparatus. FIG.2 is a partial block diagram illustrating a schematic configuration of a plural array combining section in the conventional reception apparatus. FIG.3 is a partial block diagram illustrating a schematic configuration of a propagation path estimating section in the conventional reception apparatus. FIGs.4A to 4D illustrate one example of a delay profile. FIG.5 is a partial block diagram

illustrating a schematic configuration of a Viterbi equalizer in the conventional reception apparatus. FIG.6 is a partial block diagram illustrating a schematic configuration of a replica generating section in the conventional reception apparatus.

The entire configuration of the conventional reception apparatus is first explained using FIG.1. In FIG.1, plural array combining section 12 has processing systems, of which the number is the same as that of antennas, which combine signals received at respective antennas 11, and further combines resultants weighted and then combined for each antenna.

Timing control section 13 acquires symbol synchronization timings from outputs of reception processing sections provided for each antenna in plural array combining section 12. In addition, timing control section 13 is capable of acquiring a symbol synchronization timing from an output from one of the reception processing sections.

Propagation path estimating section 14 estimates a delay profile from outputs of the reception processing sections provided for each antenna in plural array combining section 12, and recognizes a spread condition of received signal components on the time axis. That is, propagation path estimating section 14 performs propagation path estimation. In order to converge the spread of received signal components in a range enabling

delay compensation in Viterbi equalizer 16 described later, propagation path estimating section 14 calculates a time adjustment amount (τ shown in FIG.4D) for a delayed wave to output to time adjustment section 22 in plural array combining section 12. Propagation path estimating section 14 is capable of performing the propagation path estimation from an output from one of the reception processing sections.

Tap coefficient estimating section 15 estimates a coefficient that minimizes a mean square of a difference between a replica signal and a received signal (i.e., a weight based on the least square method), and outputs the estimated coefficient to feed forward filter (FFF) 23 in plural array combining section 12 and replica generating section 56 in Viterbi equalizer 16. The coefficients are used in FFF 23 and multipliers 65 to 69 in replica generating section 56.

Viterbi equalizer 16 generates the replica signal, and makes a decision on the received signal using the Viterbi algorithm with the difference between a received signal component subjected to array combining and the replica signal as likelihood information.

A configuration of plural array combining section 12 is next explained using FIG.2. While a case is explained herein, for example, where the number of array elements is 2, and the number of path groups is 2, any numbers of array elements and of path groups may be

applicable.

In FIG.2, reception processing sections 21 perform reception processing on received signals from respective antennas. Time adjustment section 22 delays a reception-processing processed received signal based on an output from propagation path estimating section 14. FFF 23 performs weighting processing on the received signal based on the tap coefficient designated from tap coefficient estimating section 15. Combining section 24 combines all the FFF processed signals of respective paths from all antennas.

A configuration of propagation path estimating section 14 is next explained using FIG.3. In FIG.3, delay profile estimating section 31 estimates a delay profile of received signals components. An example of the delay profile is illustrated in FIG.4A.

Maximum detecting section 32 detects a maximum level among power levels of the received signal components spread on the time axis in the estimated delay profile. Based on the maximum level of the power, threshold setting section 33 sets a threshold level to select only a path with excellent received condition. Any method may be applicable to determine the threshold level, for example, there is considered a method of obtaining predetermined percentages of the maximum level, or of subtracting a predetermined value from the maximum level. The delay profile with the threshold level set

is illustrated in FIG.4B.

Extracting section 34 extracts only a path with a received power level exceeding the threshold level set by threshold setting section 33. The delay profile with extracted paths is illustrated in FIG.4C.

Classifying section 35 classifies the extracted paths into groups (groups of paths). The classification is performed so that the number of states in the Viterbi algorithm becomes as small as possible in consideration of a maximum delay time enabling compensation in Viterbi equalizer 16.

For example, in FIG.4C, a delay time of a component having the greatest delay among extracted paths is 6T. Assuming herein that the maximum delay time enabling compensation in Viterbi equalizer 16 is up to 4T delay, when a received signal with the delay profile as illustrated in FIG.4C is input to Viterbi equalizer 16 without any time adjustment, reception performance deteriorates largely due to an effect of the delayed wave beyond a compensation range.

Then, when a group is determined for each 3T delay interval (every 4 components), as illustrated in FIG.4D, two groups of group A and group B are set. When time adjustment section 22 performs time adjustment on these groups later, since the delay time of the greatest delay component is 3T, signals of the groups can be efficiently equalized in Viterbi equalizer 16 capable of

compensating up to 4T delay signal.

Classifying section 35 performs the classification so as to set the number of states to be as small as possible by determining a group for each delay time interval that is as small as possible in a range allowed by a spread condition of received signal components exceeding the threshold level or as to adapt to a range enabling compensation in an equalizer. In addition, the number of groups is not limited to 2, and is determined arbitrarily.

Time adjustment amount detecting section 36 detects a time adjustment amount. That is, based on the classification result, time adjustment amount detecting section 36 detects a time amount by which each group is delayed to combine the group with the greatest delay group. For example, in this case, since the number of all the groups in FIG.4D is 2, time adjustment amount detecting section 36 detects a time adjustment amount τ of group A by which group A is combined with group B that is the greatest delay group to provide to time adjustment section 22. In other words, the time adjustment amount τ is a distance between beginning components of respective groups on the time axis. That is, the time adjustment amount τ is determined using a first wave as a reference in each group.

In addition, when there is a plurality of groups besides the greatest delay group, time adjustment amount

detecting section 36 detects the time adjustment amount for each group.

A configuration of Viterbi equalizer 16 is next explained using FIG.5. In FIG.5, subtracter 51 subtracts a replica signal from a received signal. Error power calculating section 52 calculates power corresponding to an error from the subtracted result in subtracter 51.

Viterbi calculation section 53 is, for example, comprised of an MLSE circuit that performs Maximum Likelihood Sequence Estimation, and makes a decision on a received signal using the calculated power level corresponding to the error as likelihood information.

Memory 54 stores a known signal. Switch 55 outputs the known signal stored in memory 54 to replica generating section 56 in the case of tap coefficient estimation using the known signal, while in the other case except the estimation, outputting a symbol sequence candidate output from Viterbi calculation section 53 to replica generating section 56, based on a symbol synchronization timing output from timing control section 13.

Replica generating section 56 multiplies the known signal delayed based on an output of propagation path estimating section 14 or the symbol sequence candidate of received signal by a tap coefficient estimated in tap coefficient estimating section 15, and thereby generates

a replica signal.

A configuration of replica generating section 56 is next explained using FIG.6. In FIG.6, each of delay sections 61 to 64 delays an input signal so that the reception apparatus fetches a received signal component at each sampling timing. While any number of delay sections may be applicable, the number is herein assumed to be 4. Further, assuming that a delay amount at each delay section is one symbol duration, the reception apparatus is capable of fetching up to 4T delayed wave maximum.

Each of multipliers 65 to 69 multiplies the known signal component or symbol sequence candidate by a respective tap coefficient estimated in tap coefficient estimating section 15. Delayed waves each weighted are added in adder 70. The replica signal is thereby generated.

At this point, since the tap coefficient is estimated so as to minimize the mean square of a difference between the received signal and the replica signal, it is considered that in a constitution where all the tap coefficients are estimated autonomously in tap coefficient estimating section 15, all the tap coefficients converge to 0, and that functions of the array and Viterbi equalizer are lost.

Therefore, a tap coefficient input to multiplier 65 provided at a tap corresponding to the first wave is

generally set to a fixed value (for example, 1), and under the condition that the tap coefficient to be multiplied by the first wave is 1, respective optimal tap coefficients to be multiplied by a 1T delayed wave to 4T delayed wave are estimated in tap coefficient estimating section 15, and multiplied respectively in multipliers 66 to 69.

In addition, in a replica generating section of the conventional reception apparatus, while FIG.6 illustrates the case where the tap coefficient to be multiplied by a first wave is a fixed value of 1, the fixed value is not limited to 1. In other words, any constant number that is determined to be fixed may be used as the fixed value, however, "1" providing minimum processing is often used.

Thus, the conventional reception apparatus is also designed to perform time adjustment on a delayed wave beyond a range enabling compensation in an equalizer, thereby converge a received signal component spread on a time axis in the range enabling the compensation in the equalizer, and to improve reception performance.

However, since the conventional reception apparatus combines received signals while adjusting to a first wave of each group, there is a problem that a sufficient path diversity effect is not obtained.

That is, for example, when a replica generating section is provided with 5 delay elements so that the

reception apparatus is capable of fetching up to 5T delayed wave maximum, it is possible to obtain path diversity effects corresponding to 6 paths maximum including the first wave. However, since the conventional reception apparatus combines received signals while simply adjusting to the first wave of each group to perform time adjustment, the apparatus does not always obtain the path diversity effects corresponding to 6 paths.

Disclosure of Invention

It is an object of the present invention to provide a reception apparatus and equalizing processing method capable of obtaining sufficient path diversity effects by performing path diversity always using the maximum number of paths allowed by a configuration of the apparatus without depending on a spread condition of received signal components.

To achieve the above object, in the present invention, in order for all delay elements in a replica generating section to be always employed in diversity combining, the received signal components are subjected to time adjustment corresponding to the spread condition of the received signal components on a time axis.

Brief Description of Drawings

FIG.1 is a partial block diagram illustrating a

schematic configuration of a conventional reception apparatus;

FIG.2 is a partial block diagram illustrating a schematic configuration of a plural array combining section in the conventional reception apparatus;

FIG.3 is a partial block diagram illustrating a schematic configuration of a propagation path estimating section in the conventional reception apparatus;

FIG.4A is a diagram illustrating an example of a delay profile;

FIG.4B is a diagram illustrating the example of a delay profile;

FIG.4C is a diagram illustrating the example of a delay profile;

FIG.4D is a diagram illustrating the example of a delay profile;

FIG.5 is a partial block diagram illustrating a schematic configuration of a Viterbi equalizer in the conventional reception apparatus;

FIG.6 is a partial block diagram illustrating a schematic configuration of a replica generating section in the conventional reception apparatus;

FIG.7 is a partial block diagram illustrating a schematic configuration of a reception apparatus according to one embodiment of the present invention;

FIG.8 is a partial block diagram illustrating a schematic configuration of a time adjustment amount

control section in the reception apparatus according to one embodiment of the present invention;

FIG.9 is a partial block diagram illustrating a schematic configuration of a replica generating section in the reception apparatus according to one embodiment of the present invention;

FIG.10A is a diagram illustrating an example of a delay profile of a received signal;

FIG.10B is a diagram illustrating an example of a delay profile of a received signal; and

FIG.10C is a diagram illustrating an example of a delay profile of a received signal.

Best Mode for Carrying Out the Invention

An embodiment of the present invention is explained in detail below with reference to accompanying drawings.

FIG.7 is a partial block diagram illustrating a schematic configuration of a reception apparatus according to one embodiment of the present invention. FIG.8 is a partial block diagram illustrating a schematic configuration of a time adjustment amount control section in the reception apparatus according to the embodiment of the present invention. FIG.9 is a partial block diagram illustrating a schematic configuration of a replica generating section in the reception apparatus according to the embodiment of the present invention. FIGs.10A to 10C are diagrams each illustrating an example

of a delay profile of a received signal.

The entire configuration of the reception apparatus according to this embodiment is first explained using FIG.7. In FIG.7, plural array combining section 102 has processing systems, of which the number is the same as that of antennas, which combine signals received at respective antennas 101, and further combines resultants weighted and then combined for each antenna. A configuration and function of plural array combing section 102 are the same as those of the plural array combining section of the conventional reception apparatus, and therefore the detailed explanation of plural array combining section 102 is omitted.

Timing control section 103 acquires symbol synchronization timings from outputs of reception processing sections provided for each antenna in plural array combining section 102. In addition, timing control section 103 is capable of acquiring a symbol synchronization timing from an output from one of the reception processing sections.

Propagation path estimating section 104 estimates a delay profile from outputs of the reception processing sections provided for each antenna in plural array combining section 102 to perform propagation path estimation. A configuration and function of propagation path estimating section 104 are the same as those of the propagation path estimating section in the

conventional reception apparatus, and therefore the detailed explanation of propagation path estimating section 104 is omitted. FIG.10A illustrates one example of an output of propagation path estimating section 104. In addition, propagation path estimating section 104 is capable of performing the propagation path estimation from an output from one of the reception processing sections.

Time adjustment amount control section 105 detects the number of combined signal components to be generated when the received signal components are converged based on a time adjustment amount calculated in propagation path estimating section 104. Then, time adjustment amount control section 105 compares the number of combined signal components to be generated with the number of delay elements of the replica generating section in Viterbi equalizer 107 described later, and when the numbers are different, resets a time adjustment amount to be instructed to a time adjustment section in plural array combining section 102 so that the numbers accord with each other, which is described later in detail.

Tap coefficient estimating section 106 estimates a coefficient that minimizes a mean square of a difference between a replica signal and a received signal (i.e., a weight based on the least square method), and outputs the estimated coefficient to FFF in plural array

combining section 102 and the replica generating section in Viterbi equalizer 107. The coefficients are used in the FFF and multipliers 305 to 309 in the replica generating section.

Viterbi equalizer 107 generates the replica signal, and makes a decision using the Viterbi algorithm with the difference between the replica signal and a received signal component subjected to the time adjustment and then to array combining as likelihood information.

A configuration of time adjustment amount control section 105 is next explained using FIG.8. In FIG.8, temporary combining section 201 converges received signal components to combine based on the time adjustment amount (e.g., time between first waves of respective groups) calculated by propagation path estimating section 104.

Spread condition detecting section 202 detects a spread condition of received signal components. Further, spread condition detecting section 202 calculates a symbol delay up to which exists on combined signal components from the combined result in temporary section 201.

Time adjustment amount resetting section 203 determines whether or not the delay elements of the replica generating section in Viterbi equalizer 107 are all used when the received signal components are converged as instructed from propagation path estimating

section 104, using the spread condition of the received signal components, a time spread (symbol lengths where the combined signal components exist) of the combined signal components to be generated when the received signal components are converged as instructed from propagation path estimating section 104, and the maximum delay amount enabling the compensation in Viterbi equalizer 107.

That is, time adjustment amount resetting section 203 determines whether or not the number of combined received signal components accords with the number of delay elements in the replica generating section. Then, when the numbers are out of accordance with each other, time adjustment amount resetting section 203 calculates a time adjustment amount such that the numbers are in accordance with each other, and outputs the calculated time adjustment amount to the time adjustment section in plural array combining section 102.

In other words, time adjustment amount resetting section 203 calculates the time adjustment amount such that a sampling timing of a greatest delay component among extracted received signal components accords with the maximum delay time enabling the compensation in Viterbi equalizer 107.

A configuration of the replica generating section in Viterbi equalizer 107 is next explained using FIG.9. In FIG.9, each of delay sections 301 to 304 delays an

input signal so that the reception apparatus fetches the received signal component at each sampling timing. While any number of delay sections may be applicable, the number is assumed herein to be 4. When it is assumed that a delay amount of each delay section is one symbol duration, the reception apparatus is capable of fetching up to 4T delayed wave maximum.

Each of multipliers 305 to 309 multiplies a known signal component or symbol sequence candidate by the tap coefficient estimated in tap coefficient estimating section 106. In addition, in order for all the tap coefficients not to converge to 0, the tap coefficient to be multiplied by a first wave is set at a fixed value (herein, 1). Delayed waves each weighted by the respective tap coefficient are added in adder 301. The replica signal is thereby generated.

As illustrated in FIG.9, in the replica generating section of the reception apparatus according to this embodiment, all the delay sections 301 to 304 are always used. Accordingly, it is possible to obtain increased path diversity effects, and to improve the reception performance.

The operation of the reception apparatus with the above configuration is next explained.

A signal undergoing various distortions in a propagation path is received at antenna 101. Plural array combining section 102 performs reception

processing on a received signal. Timing control section 103 detects a symbol synchronization timing using the reception-processing processed received signal.

Propagation path estimating section 104 performs propagation path estimation using the reception-processing processed received signal. Further, in order to converge spread received signal components in the range enabling the compensation in Viterbi equalizer 107, propagation path estimating section 104 estimates a time adjustment amount for a delayed wave.

The estimated time adjustment amount is corrected by time adjustment amount control section 105 so that the delay elements of the replica generating section in Viterbi equalizer 107 are all used.

FIG.10A illustrates a time adjustment amount τ estimated in propagation path estimating section 104. At this point, in order to combine group A and group B, a distance on the time axis between a beginning component of group A and a beginning component of group B is estimated as the time adjustment amount τ.

Then, based on the time adjustment amount τ, temporary combining section 201 in time adjustment amount control section 105 combines delayed waves of respective groups. FIG.10B illustrates combinations of respective delayed waves of groups A and B. Using the combined result, spread condition detecting section 202 detects a delay amount of the greatest delayed wave, and

compares the detected maximum delay with the number of delay elements of the replica generating section. At this point, as illustrated in FIG.10B with the result of temporary combining, the maximum delay is 3T, the number of delay elements 301 to 304 in the replica generating section is 4, and therefore delay element 304 is not used when the time adjustment amount is maintained. Accordingly, the path diversity is not obtained sufficiently, and it is thereby judged that resetting is needed of the time adjustment amount to be instructed to the time adjustment section in plural array combining section 102.

When it is judged that the resetting of the time adjustment amount is needed, time adjustment amount resetting section 203 adds or subtracts unit delay time T to/from the time adjustment amount τ, and thereby calculates a time adjustment amount τ' such that the maximum delay of the combined signal components accords with the number of delay elements in the replica generating section. In addition, the unit delay time T is determined corresponding to a delay amount in each delay section. Accordingly, when the delay amount in each delay section is one symbol duration, the addition or subtraction is performed based on one symbol duration, while when the delay amount in each delay section is 1/2 symbol duration, the addition or subtraction is performed based on 1/2 symbol duration.

In the case illustrated in FIG.10B, when τ' is made equal to τ-T ($\tau'=\tau$-T), as illustrated in FIG.10C, it is possible to accord the maximum delay with the number of delay elements in the replica generating section. Therefore, the new time adjustment amount $\tau'=\tau$-T is output to the time adjustment section in plural array combining section 102.

The reception-processing processed received signal is subjected to time adjustment based on the corrected time adjustment amount that is an output of time adjustment amount control section 105, and further is subjected to array combining at each sampling timing.

A difference between the received signal and the replica signal calculated in Viterbi equalizer 107 is provided to tap coefficient estimating section 106. Then, tap coefficient estimating section 106 estimates a new tap coefficient so as to minimize the mean square of the difference between the received signal and the replica signal. The estimated tap coefficient is provided to Viterbi equalizer 107. The tap coefficient in the replica generating section in Viterbi equalizer 107 is thereby updated.

Thus, according to this embodiment, the time adjustment of received signal components is performed corresponding to the spread condition of the received signal component on the time axis so that delay sections that a replica generating section has are all used at

the time of diversity combining, whereby it is possible to perform the path diversity always using the maximum number of paths allowed by an apparatus configuration.

In addition, while this embodiment explains the configuration using a plurality of adaptive array antennas, the present invention is not limited to this condition. That is, this embodiment may be applicable to a case of using a signal adaptive array antenna and another case of using an ordinary antenna instead of using the adaptive array antenna.

Further, in this embodiment, it may be possible to make a tap position variable to which a fixed value is input at the time a replica signal is generated, corresponding to a received level of a received signal component.

As described above, according to the present invention, it is possible to perform path diversity always using the maximum number of paths allowed by an apparatus configuration, whereby it is possible to improve the diversity effect, and to improve the error rate.

This application is based on the Japanese Patent Application No.HEI11-152301 filed on May 31, 1999, entire content of which is expressly incorporated by reference herein.

Industrial Applicability

The present invention is applicable to a base station apparatus used in a radio communication system, and further is applicable to a communication terminal apparatus performing a radio communication with the base station apparatus.

CLAIMS

1. A reception apparatus comprising:

a combiner that combines a predetermined number of signal components spread on a time axis after performing weighting on the components;

a converger that converges received signal components spread on the time axis in a range which enables signals in the range to be combined in the combiner; and

a controller that controls the converger so that a sampling timing of a signal component with a greatest delay amount among converged received signal components accords a maximum delay time in the range enabling signals in the range to be combined in the combiner.

2. The reception apparatus according to claim 1, wherein the controller controls the converger so as to generate a same number of signal components as that of delay elements that the combiner has.

3. The reception apparatus according to claim 1, further comprising:

a plurality of adaptive array antennas that receives signals incoming in predetermined respective directions; and

an array receiver that adds signals received at respective adaptive array antennas after performing weighting on the signals.

4. A communication terminal apparatus mounted with a

reception apparatus, said reception apparatus comprising:

a combiner that combines a predetermined number of signal components spread on a time axis after performing weighting on the components;

a converger that converges received signal components spread on the time axis in a range which enables signals in the range to be combined in the combiner; and

a controller that controls the converger so that a sampling timing of a signal component with a greatest delay amount among converged received signal components accords a maximum delay time in the range enabling signals in the range to be combined in the combiner.

5. A base station apparatus that performs a radio communication with the communication terminal apparatus according to claim 4.

6. A base station apparatus mounted with a reception apparatus, said reception apparatus comprising:

a combiner that combines a predetermined number of signal components spread on a time axis after performing weighting on the components;

a converger that converges received signal components spread on the time axis in a range which enables signals in the range to be combined in the combiner; and

a controller that controls the converger so that

a sampling timing of a signal component with a greatest delay amount among converged received signal components accords a maximum delay time in the range enabling signals in the range to be combined in the combiner.

7. A communication terminal apparatus that performs a radio communication with the base station apparatus according to claim 6.

8. An equalizing processing method comprising:

a combining step of combining a predetermined number of signal components spread on a time axis after performing weighting on the components;

a converging step of converging received signal components spread on the time axis in a range which enables signals in the range to be combined at the combining step; and

a controlling step of controlling the converging step so that a sampling timing of a signal component with a greatest delay amount among converged received signal components accords a maximum delay time in the range enabling signals in the range to be combined at the combining step.

ABSTRACT

Time adjustment amount control section 105 detects a time span amount of combined received signals to be generated when received signal components are converged based on a time adjustment amount calculated in propagation path estimating section 104, compares the time span amount with the number of delay elements of a replica generating section in Viterbi equalizer 107, and when the amount does not accord with the number, resets the time adjustment amount to instruct to a time adjustment section in plural array combining section 102 so that the amount accords with the number.

11
12
PLURAL ARRAY COMBINING SECTION
13
TIMING CONTROL SECTION
14
PROPAGATION PATH ESTIMATING SECTION
15
TAP COEFFICIENT ESTIMATING SECTION
16
VITERBI EQUALIZER

FIG. 1

FIG.2

FIG.3

FIG.4A

FIG.4B

FIG.4C

FIG.4D

FROM PLURAL ARRAY COMBINING SECTION 12
51
REPLICA GENERATING SECTION
56
ERROR POWER CALCULATING SECTION
52
VITERBI CALCULATION SECTION
53
55
MEMORY
54
FROM PROPAGATION PATH ESTIMATING SECTION 14
FROM/TO TAP COEFFICIENT ESTIMATING SECTION 15
FROM TIMING CONTROL SECTION 13

FIG.5

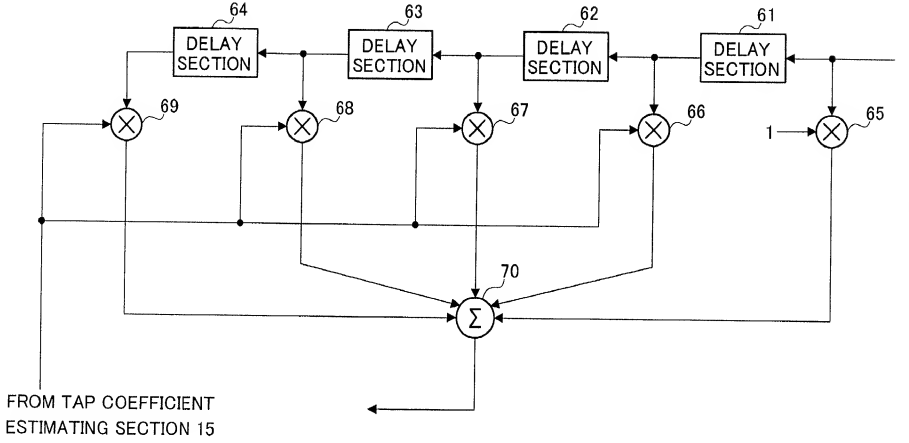

FIG.6

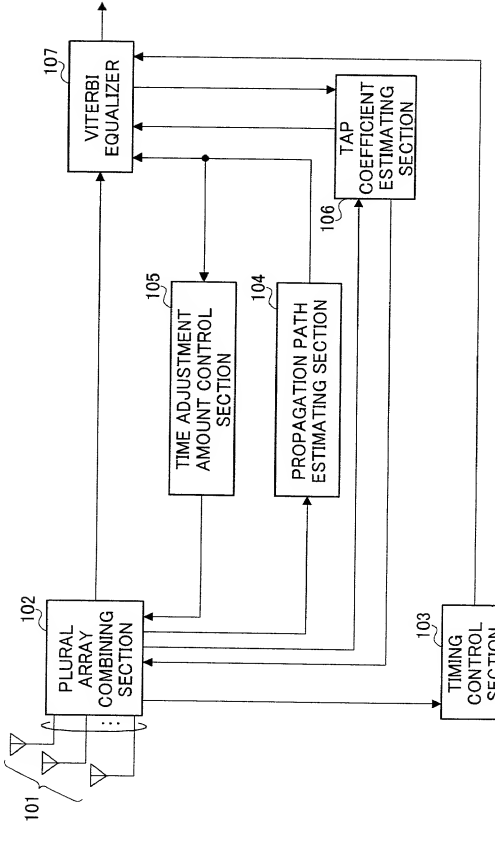
101
102
PLURAL ARRAY COMBINING SECTION
103
TIMING CONTROL SECTION
104
PROPAGATION PATH ESTIMATING SECTION
105
TIME ADJUSTMENT AMOUNT CONTROL SECTION
106
TAP COEFFICIENT ESTIMATING SECTION
107
VITERBI EQUALIZER

FIG. 7

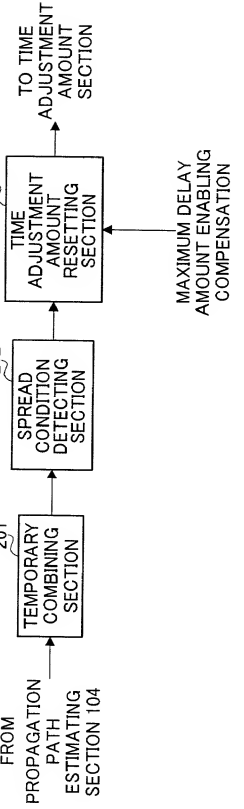
FROM PROPAGATION PATH ESTIMATING SECTION 104
201
TEMPORARY COMBINING SECTION
202
SPREAD CONDITION DETECTING SECTION
203
TIME ADJUSTMENT AMOUNT RESETTING SECTION
TO TIME ADJUSTMENT AMOUNT SECTION
MAXIMUM DELAY AMOUNT ENABLING COMPENSATION

FIG.8

FIG.9

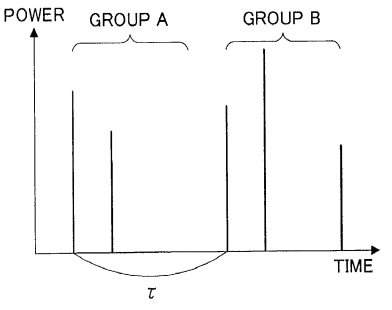

FIG.10A

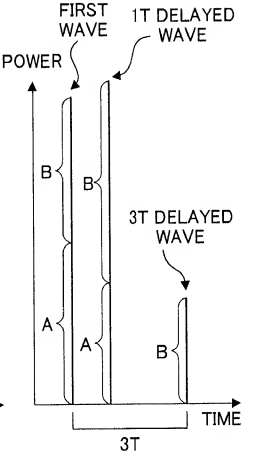

FIG.10B

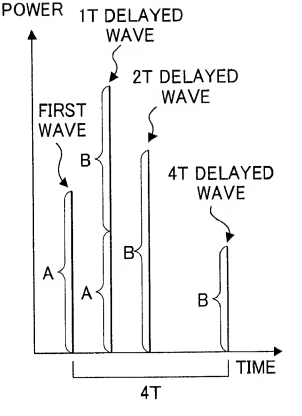

FIG.10C

APPLICATION FOR UNITED STATES PATENT
Declaration for Patent Application

As a below named inventor, I hereby declare that:
My residence, post office address and citizenship are as stated below next to my name.
I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on

the invention entitled: RECEPTION APPARATUS AND EQUALIZING PROCESSING METHOD

the specification of which 2 (file no _____)

(check at least one) 3 [X] is attached hereto
4 [ ] was filed on _____ as (5) U.S. Application Serial No. _____
6 [ ] and was amended _____ (if applicable)

Use this portion only if you are entering the U.S. National phase based on a PCT International Application designating the U.S.

7 [x] was filed as PCT international application
8 Number **PCT/JP00/03446**
9 on **May 30, 2000**
and was amended under PCT Article(s) 19 and/or 34
10 on _____ (if applicable).

I hereby declare that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended, by any amendment referred to above.
I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me which is material to patentability in accordance with Title 37, Code of Federal Regulations, §1.56.
I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application (s) for patent or inventor's certificate listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date earlier than that of the application(s) on which priority is claimed.

Prior (Foreign) Application(s) any Priority Claims Under 35 U.S.C. 119 — Priority Claimed

11a	**JAPAN** (Country)	**JP11-152301** (Number)	**31/05/1999** (Day/Month/Year Filed)	[x] Yes	[ ] No
	_____ (Country)	_____ (Number)	_____ (Day/Month/Year Filed)	[ ] Yes	[ ] No

[ ] Additional foreign application numbers are listed on a supplemental priority data sheet attached hereto.

Priority Claim(s) from U.S. Provisional Application(s) – I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States provisional application(s) listed below:

11b	_____ Application No.	_____ Day/Month/Year Filed	_____ Application No.	_____ Day/Month/Year Filed

Do not use this portion to identify a PCT application if the parent application is the U.S. National phase of the PCT application

I hereby claim the benefit under Title 35, United States Code, 120 of any United States application(s) or PCT international application(s) designating the United States of America that is/are listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code §112, I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between filing date of the prior application and the national or PCT international filing date of this application.

13	_____ (U.S. Application Number)	_____ (U.S. Filing Date)	_____ Status (patented, pending, abandoned)

I hereby appoint the following attorneys of the firm of Stevens, Davis, Miller & Mosher, L.L.P. as my attorneys of record with full power of substitution and revocation to prosecute this application and to transact all business in the Patent and Trademark Office:

James E. Ledbetter, Reg. No. ~~28732;~~ Thomas P. Pavelko, Reg. No. ~~31689;~~ and Anthony P. Venturino, Reg. No. 31674.

ALL CORRESPONDENCE IN CONNECTION WITH THIS APPLICATION SHOULD BE SENT TO STEVENS, DAVIS, MILLER & MOSHER, L.L.P., 1615 L Street, N.W., Suite 850, Washington, D.C. 20036, TELEPHONE (202) 408-5100, FACSIMILE (202) 408-5200.

See page 2 for signature lines

other side for instructions for completing this form

STEVENS, DAVIS, MILLER & MOSHER, L.L.P.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful statements may jeopardize the validity of the application or any patent issuing thereon.

PAGE 2 OF U.S.A. DECLARATION FORM

13a	Typewritten Full Name of Sole or First Inventor	**Yoshiko**		**SAITO**
		Given Name	Middle Name	Family Name
14a	Inventor's Signature	Yoshiko		Saito
15a	Date of Signature	October	13,	2000
		Month	Day	Year
16a	Residence	**Yokosuka-shi**	**Kanagawa**	**JAPAN**
		City	State or Province	Country
17a	Citizenship	**JAPAN**		JPX
18a	Post Office Address *(Insert complete mailing address, including country)*	**4-3-20-301, Ikeda-cho,**		
		Yokosuka-shi, Kanagawa 239-0806 JAPAN		
13b	Typewritten Full Name of Sole or Second Inventor	**Mitsuru**		**UESUGI**
		Given Name	Middle Name	Family Name
14b	Inventor's Signature	Mitsuru		Uesugi
15b	Date of Signature	October	13,	2000
		Month	Day	Year
16b	Residence	**Yokosuka-shi**	**Kanagawa**	**JAPAN**
		City	State or Province	Country
17b	Citizenship	**JAPAN**		JPX
18b	Post Office Address *(Insert complete mailing address, including country)*	**17-1-402, Anjindai,**		
		Yokosuka-shi, Kanagawa 238-0048 JAPAN		
13c	Typewritten Full Name of Sole or Third Inventor			
		Given Name	Middle Name	Family Name
14c	Inventor's Signature			
15c	Date of Signature			
		Month	Day	Year
16c	Residence			
		City	State or Province	Country
17c	Citizenship			
18c	Post Office Address *(Insert complete mailing address, including country)*			
13d	Typewritten Full Name of Sole or Fourth Inventor			
		Given Name	Middle Name	Family Name
14d	Inventor's Signature			
15d	Date of Signature			
		Month	Day	Year
16d	Residence			
		City	State or Province	Country
17d	Citizenship			
18d	Post Office Address *(Insert complete mailing address, including country)*			

*Note to Inventor: Please sign name on line 15 exactly as it appears in line 14 and insert the actual date of signing on line 16. If there are more than four inventors, please add a copy of this page for identification and signatures for the additional inventors.

INSTRUCTIONS FOR COMPLETION OF THIS FORM

line 1 Insert the same title as is used on the specification and in the assignment.

line 2 Is optional but is provided so that you can use it to identify more readily an application prior to the time that the Patent Office application serial number is assigned. We suggest that the specification, drawings and declaration always bear a file number since it can help to get the papers together in case they become inadvertently separated. In instances where the specification is filed without a signed declaration form (under 37 CFR §1.53) a file number on a later-received separate form will assist us in associating it with the correct case.

line 3 Check this box if the specification, claims and drawing (if any) are attached to this declaration form, e.g., when filing a new patent application.

lines 4-5 Are only used in an instance where the application is already on file and the declaration from is being separately filed, e.g., when the application was originally filed without a signed declaration or where the Patent Office has required a new declaration because of a deficiency in the original declaration. In such an instance the Patent Office will require that lines 4 and 5 be completed with the filing date and application serial number already assigned.

line 6 Is used in conjunction with line 5 but only when there have been one or more amendments to the specification or claims. Line 6 is also used when the Examiner requires a new declaration because claims inserted by amendment cover subject matter not originally claimed (37 CFR §1.67).

lines 7-10 Are for PCT (Patent Cooperation Treaty) cases and are used only when you are entering the U.S. National phase (Chapter I or II) based upon a previously filed PCT International application designating the U.S.

line 7 Check this box if this is a PCT National Phase application.

line 8 Insert PCT International application number.

line 9 Insert date of filing of PCT International application.

lines 10 Insert the date of all amendments filed in the PCT International application. Such amendments are optional, so this line at times will not be used.

line 11a Is used in the following instances:

(i) If a single priority is being claimed from a foreign application you need to list only the first-filed application; you do not need to list other countries if all applications were filed within one year of the U.S. filing.

(ii) If multiple priorities are being claimed, from a plurality of applications filed in one or more countries, you must list the first filed application for each aspect of the invention. Example: if aspect A of the invention was disclosed in an application filed 11 months earlier in country X and aspect B was disclosed 9 months earlier in an application filed in country Y, then the applications in both countries X and Y must be identified. Only the first application for each aspect of the invention needs to be identified provided all applications on that aspect were filed within one year prior to the U.S. filing.

(iii) If a non-priority application is being filed you must list all applications in all countries where corresponding foreign applications were filed more than one year prior to the U.S. filing. This is so the Examiner can check to see if any of those applications were published or patented early enough to be prior art against the U.S. application.

(iv) If there are more than two applications to be listed we suggest that you type in on this form only "See attached Schedule A" and then list all of the previous applications on an attached sheet.

line 11b Is used to claim priority under 35 USC §119(e) based on a provisional application filed within one year of the filing of the instant application. More than one provisional application may be identified provided neither was filed more than one year earlier.

line 12 This block is used only in instances where there is a previously filed U.S. non-provisional application which was copending at the time the present application was (or is being) filed. that previous application could be a U.S. non-provisional application or the National Phase of a PCT allocation. In such a case the present application may be entitled to the priority of the previous application's U.S. filing date (and consequently the foreign priority thereof) provided the present application is identified as a continuing application (continuation, divisional or continuation-in-part) of the earlier (parent) application. If the foregoing is applicable, please fill in one line for each such prior application.

line 13 Type the inventor's proper legal name in the order specified, e.g., "John B. JONES" or "J. Bob JONES" if the inventor so prefers. It is not acceptable to use only initials such as "J. B. JONES."

line 14 The inventor's "signature" may be his (or her) usual manner of signing but it is preferable that the inventor simply write his (or her) name in his (or her) own cursive handwriting in the same order as on line 14, e.g., given name, middle initial and Family name.

line 15 Insert the actual date of signature.

line 16 Insert simply the city and state or country, e.g., "Paris, France", of the inventor's residence, not citizenship. No street address or postal code is required on this line.

line 17 Insert the inventor's citizenship. The statement of citizenship (or subject of) is a statutory requirement (35 USC §115). Simply the name of the country of citizenship, e.g., "Japan" is sufficient.

line 18 Insert the inventor's mailing address. The purpose of requiring the post office address is to enable the Patent Office to communicate directly with the inventor if desired, such as in the case of death of the U.S. attorney. It should be the address where the inventor customarily receives his (or her) mail and should include the postal code. If applicable it can be the inventor's business address or address at place of employment.

Applicants are reminded that the U.S. Patent and Trademark Office has very strict requirements as to proper execution of an application. The applicant should make sure that he reviews the declaration, prior to signing to make sure the declaration properly identifies the application and all relevant information; and should review the specification and claims (including drawings, if any) before signing the declaration. Failure to do so will require the filing of a supplemental declaration --- 37 CFR §1.67(c)

Any handwritten changes to the specification, claims or drawings must be in ink personally by all of the inventors prior to signing the declaration and the adjacent left margin must be initialed and dated by all of the inventors, e.g., "JBJ 6-9-91".

Please let us know if there are any questions regarding proper completion of this form. Thank you.

An assignment, a separate document requiring separate signature and dating may be enclosed. Please look for it and sign and date it in the same manner as in lines 15 and 16 above.